UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,989	01/30/2001	John Xiaoxiong Zhong	004162.P004	4365

35273 7590 05/21/2004

BEVER, HOFFMAN & HARMS, LLP
1432 CONCANNON BLVD
BLDG G
LIVERMORE, CA 94550-6006

EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/21/2004 8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/774,989	Applicant(s) ZHONG, JOHN XIAOXIONG	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *April 2, 03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 of the application have been examined.

Drawings

2. The drawings submitted on January 30, 2001 are accepted.

Specification

3. The disclosure is objected to because of the following informalities:

Page 6, Lines 11-12, "a circuit with n elements could be represented and simulated with data structures that are asymptotically smaller than (e.g., $\log_2(n)$)" appears to be incorrect and it appears that it should be "a circuit with n elements could be represented and simulated with data structures that are asymptotically smaller than n (e.g., $\log_2(n)$)".

Page 10, Line 11, "If l = log2(n+1)" appears to be incorrect and it appears that it should be "If l = $\log_2(n+1)$".

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-8, 10-20 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tcherniaev et al.** (U.S. Patent 6,577,992) in view of **Bogliolo et al.** (IEEE, 1995: "Reliability Evaluation of Combinational logic circuits by symbolic simulation"), and further in view of **Clarke et al.** (IEEE, 1996: "Computer-aided verification").

6.1 **Tcherniaev et al.** teaches Transistor level circuit simulator using hierarchical data. Specifically, as per claim 13, **Tcherniaev et al.** teaches an apparatus of simulating a circuit (CL1, L7-11; CL2, L64 to CL3, L4; Fig. 1); comprising:

means for representing a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single

instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the outputs associated with all of the plurality of identical components (CL3, L35-41; CL3, L50-55; CL3, L60-66; CL4, L17-38; Fig. 2C; Fig. 2D).

Tcherniaev et al. does not expressly teach means for symbolically simulating the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components. **Bogliolo et al.** teaches means for symbolically simulating the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components (Page 235, CL1, Abstract; Page 237, CL2, Para 2 to Page 238, CL1, Para 1), because as per **Clarke et al.** checking the formulas depends not on the number of states of the model, but on the compactness of the symbolic forms (Page 653, CL2, Para 6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the apparatus of **Tcherniaev et al.** with the apparatus of **Bogliolo et al.** that included means for symbolically simulating the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components. One would be motivated because checking the formulas would depend not on the number of states of the model, but on the compactness of the symbolic forms.

6.2 As per claims 14 and 15, **Tcherniaev et al., Bogliolo et al.** and **Clarke et al.** teach the apparatus of Claim 13. **Tcherniaev et al.** does not expressly teach that the circuit comprises n signals having 2^n states, and encoding the circuit produces simulation run time data structures

asymptotically smaller than n; and the circuit comprises n signals having 2^n states, and encoding the circuit produces simulation run time data structures asymptotically close to log(n). **Clarke et al.** teaches that the circuit comprises n signals having 2^n states, and encoding the circuit produces simulation run time data structures asymptotically smaller than n; and the circuit comprises n signals having 2^n states, and encoding the circuit produces simulation run time data structures asymptotically close to log(n) (Page 65, CL2, Para 4 to Para 6), because checking the formulas depends not on the number of states of the model, but on the compactness of the symbolic forms (Page 65, CL2, Para 6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the apparatus of **Tcherniaev et al.** with the apparatus of **Clarke et al.** that included the circuit comprising n signals having 2^n states, and encoding the circuit producing simulation run time data structures asymptotically smaller than n; and the circuit comprising n signals having 2^n states, and encoding the circuit producing simulation run time data structures asymptotically close to log(n). One would be motivated because checking the formulas would depend not on the number of states of the model, but on the compactness of the symbolic forms.

6.3 As per claim 16, **Tcherniaev et al.** teaches that each input port of the reduced form of the circuit is mapped to an encoded port and each output value is decoded back to a set of values of outputs of the plurality of identical components, where each value in the set of values corresponds to an output of one of the plurality of identical components (CL3, L35-41; CL3, L50-55; CL3, L60-66; CL4, L17-38; Fig. 2C; Fig. 2D).

6.4 As per claims 17-19, **Tcherniaev et al.** teaches that each input i of the single instance of the identical. subcircuit in the reduced form of each input i represents the input i for all of the plurality of identical subcircuits (CL4, L12-27); each output i of the single instance of the identical component in the reduced form represents the output i for each component in the plurality of identical components (CL4, L12-38); and each component in the plurality of identical components comprises a plurality of identical subcircuits, and the single instance of the identical component in the reduced form includes a single instance of the identical subcircuit (CL3, L35-41; CL3, L50-55).

6.5 As per claim 20, **Tcherniaev et al., Bogliolo et al.** and **Clarke et al.** teach the apparatus of Claim 13. **Tcherniaev et al.** does not expressly teach that input encoding in the reduced form is generated by applying binary encoding to inputs of the plurality of identical components. **Clarke et al.** teaches that input encoding in the reduced form is generated by applying binary encoding to inputs of the plurality of identical components (Page 65, CL2, Para 5; Page 65, CL1, Para 4), because binary encoding and binary decision diagrams make it easier to manipulate during analysis and model checking (Page 65, CL2, Para 5). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the apparatus of **Tcherniaev et al.** with the apparatus of **Clarke et al.** that included input encoding in the reduced form being generated by applying binary encoding to inputs of the plurality of identical components. One would be motivated because binary encoding and binary decision diagrams would make it easier to manipulate during analysis and model checking.

6.6 As per claim 22, **Tcherniaev et al., Bogliolo et al.** and **Clarke et al.** teach the apparatus of Claim 13. **Tcherniaev et al.** does not expressly teach that symbolically simulating the reduced form of the circuit is performed using Binary Decision Diagram (BDD). **Bogliolo et al.** teaches that symbolically simulating the reduced form of the circuit is performed using Binary Decision Diagram (BDD) (Page 235, CL1, Abstract; Page 237, CL2, Para 2 to Page 238, CL1, Para 1), because as per **Clarke et al.** binary encoding and binary decision diagrams make it easier to manipulate during analysis and model checking (Page 65, CL2, Para 5).. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the apparatus of **Tcherniaev et al.** with the apparatus of **Bogliolo et al.** that included symbolically simulating the reduced form of the circuit being performed using Binary Decision Diagram (BDD). One would be motivated because binary encoding and binary decision diagrams would make it easier to manipulate during analysis and model checking.

6.7 As per claims 23 and 24, **Tcherniaev et al.** teaches that the components comprise one or more selected from the group consisting of a net, a port, an array, and a memory (CL3, L35-41); and at least one of the components comprises at least one signal having a plurality of states (CL4, L12-27).

6.8 As per Claims 1-8 and 10-12, these are rejected based on the same reasoning as Claims 13-20 and 22-24, supra. Claims 1-8 and 10-12 are method claims reciting the same limitations as Claims 13-20 and 22-24, as taught throughout by **Tcherniaev et al., Bogliolo et al.** and **Clarke et al.**

6.8 As per Claim 25, it is rejected based on the same reasoning as Claim 13, supra. Claim 25 is an article of manufacture claim reciting the same limitations as Claim 13, as taught throughout by **Tcherniaev et al., Bogliolo et al.** and **Clarke et al.**

7. Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tcherniaev et al.** (U.S. Patent 6,577,992) in view of **Bogliolo et al.** (IEEE, 1995: "Reliability Evaluation of Combinational logic circuits by symbolic simulation"), and further in view of **Clarke et al.** (IEEE, 1996: "Computer-aided verification") and **Sangiovanni et al.** (ACM, 1996: "Verification of Electronic systems").

7.1 As per claim 21, **Tcherniaev et al., Bogliolo et al.** and **Clarke et al.** teach the apparatus of Claim 13. **Tcherniaev et al.** does not expressly teach that input encoding in the reduced form is generated by applying ternary encoding to inputs of the plurality of identical components. **Sangiovanni et al.** teaches that input encoding in the reduced form is generated by applying ternary encoding to inputs of the plurality of identical components (Page 65, CL2, Para 5; Page 65, CL1, Para 4), because as per **Clarke et al.** ternary encoding makes it easier to manipulate during analysis and model checking (Page 65, CL2, Para 5). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the apparatus of **Tcherniaev et al.** with the apparatus of **Sangiovanni et al.** that included input encoding in the reduced form being generated by applying ternary encoding to inputs of the plurality of identical

components. One would be motivated because ternary encoding would make it easier to manipulate during analysis and model checking.

7.2 As per Claim 9, it is rejected based on the same reasoning as Claim 21, supra. Claims 9 is a method claim reciting the same limitations as Claim 21, as taught throughout by **Tcherniaev et al., Bogliolo et al., Clarke et al.** and **Sangiovanni et al.**

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
May 15, 2004

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100